# PATENT COOPERATION TREATY

# PCT

## INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

| | | |
|---|---|---|
| Applicant's or agent's file reference<br>P100553 | **FOR FURTHER ACTION** | See Form PCT/IPEA/416 |
| International application No.<br>**PCT/SG2004/000356** | International filing date *(day/month/year)*<br>26 October 2004 | Priority date *(day/month/year)*<br>31 October 2003 |
| International Patent Classification (IPC) or national classification and IPC<br>**Int. Cl.** [7] G11C 11/15 | | |
| Applicant<br>AGENCY FOR SCIENCE, TECHNOLOGY AND RESEARCH et al | | |

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 3 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. [X] *(sent to the applicant and to the International Bureau)* a total of **6** sheets, as follows:
      - [ ] sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      - [ ] sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.

   b. [ ] *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or table related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

| | | |
|---|---|---|
| [X] | Box No. I | Basis of the report |
| [ ] | Box No. II | Priority |
| [ ] | Box No. III | Non-establishment of opinion with regard to novelty, inventive step and industrial applicability |
| [ ] | Box No. IV | Lack of unity of invention |
| [X] | Box No. V | Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement |
| [ ] | Box No. VI | Certain documents cited |
| [ ] | Box No. VII | Certain defects in the international application |
| [ ] | Box No. VIII | Certain observations on the international application |

| | |
|---|---|
| Date of submission of the demand<br>~~31~~ August 2005 | Date of completion of the report<br>20 September 2005 |
| Name and mailing address of the IPEA/AU<br>AUSTRALIAN PATENT OFFICE<br>PO BOX 200, WODEN ACT 2606, AUSTRALIA<br>E-mail address: pct@ipaustralia.gov.au<br>Facsimile No. (02) 6285 3929 | Authorized Officer<br>**J.W. THOMSON**<br>Telephone No. (02) 6283 2214 |

# INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
**PCT/SG2004/000356**

**Box No. I Basis of the report**

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:

   ☐ international search (under Rules 12.3 and 23.1 (b))

   ☐ publication of the international application (under Rule 12.4)

   ☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements** of the international application, this report is based on (*replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report*):

   ☐ the international application as originally filed/furnished

   ☒ the description:

   pages **1 - 16** as originally filed/furnished
   pages* received by this Authority on with the letter of
   pages* received by this Authority on with the letter of

   ☒ the claims:

   pages as originally filed/furnished
   pages* as amended (together with any statement) under Article 19
   pages* **17 - 22** received by this Authority on **29 August 2005** with the letter of **29 August 2005**
   pages* received by this Authority on with the letter of

   ☒ the drawings:

   pages **1 - 12** as originally filed/furnished
   pages* received by this Authority on with the letter of
   pages* received by this Authority on with the letter of

   ☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing.

3. ☐ The amendments have resulted in the cancellation of:

   ☐ the description, pages
   ☐ the claims, Nos.
   ☐ the drawings, sheets/figs
   ☐ the sequence listing (*specify*):
   ☐ any table(s) related to the sequence listing (*specify*):

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

   ☐ the description, pages
   ☐ the claims, Nos.
   ☐ the drawings, sheets/figs
   ☐ the sequence listing (*specify*):
   ☐ any table(s) related to the sequence listing (*specify*):

* *If item 4 applies, some or all of those sheets may be marked "superseded."*

# INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
**PCT/SG2004/000356**

**Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

| | | | |
|---|---|---|---|
| Novelty (N) | Claims | 1 - 26 | **YES** |
| | Claims | | **NO** |
| Inventive step (IS) | Claims | 1 - 26 | **YES** |
| | Claims | | **NO** |
| Industrial applicability (IA) | Claims | 1 - 26 | **YES** |
| | Claims | | **NO** |

2. Citations and explanations (Rule 70.7)

US 2004/0125646.

EP 1339065

WO 2002/059973

US 2002/0036917

**Novelty and Inventive Step – claims 1 to 26**

The invention as defined in claims 1 to 26 is not disclosed in the above citations. The differences between the disclosures of the citations and the claimed invention involve an inventive step.

Claims 1 to 26 are therefore novel and involve an inventive step. The claimed invention has industrial applicability.

**CLAIMS**

What is claimed is:

1. A magnetoresistive random access memory (MRAM) unit comprising:

a substrate;

a plurality of transistors formed on said substrate, each of said plurality of transistors being a field-effect transistor comprising a first source/drain electrode, a second source/drain electrode and a gate electrode;

a plurality of active areas defined in a common memory block comprising a ferromagnetic recording layer, a free magnetic reading layer, a non-magnetic space layer between said ferromagnetic recording layer and said free magnetic reading layer~~, and a plurality of active areas defined in said common memory block~~;

a plurality of contacts, each of said plurality of contacts electrically connecting a respective one of said first source/drain electrodes with a corresponding one of said plurality of active areas; and

a common electrode in electrical contact with said plurality of contacts through said common memory block, said common electrode serving as bit line for said first source/drain electrodes;

wherein each of said plurality of active areas forms an effective magnetoresistive element; and

wherein each of said plurality of transistors is controllable to electrically activate a corresponding one of said plurality of contacts and thereby to write/read a data bit into/from said ferromagnetic recording layer at a respective one of said effective magnetoresistive elements.

2. The MRAM unit as claimed in claim 1, wherein said corresponding one of said plurality of contacts is electrically activatable by means of electrically connecting said respective one of said first source/drain electrodes with said corresponding second source/drain electrode.

3. The MRAM unit as claimed in claim 1, wherein a plurality of bit lines is in electrical contact with said second source/drain electrodes.

4. The MRAM unit as claimed in claim 1, wherein a plurality of word lines is in electrical contact with said gate electrodes.

5. The MRAM unit as claimed in claim 1, wherein a common auxiliary electrode is provided in electrical contact between said common electrode and said common memory block.

6. The MRAM unit as claimed in claim 1, wherein a common digital line is provided next to said common electrode on an opposite side of said common electrode with respect to said common memory block.

7. The MRAM unit as claimed in claim 6, wherein said common digital line is electrically insulated from said common electrode.

8. The MRAM unit as claimed in claim 1, wherein said ferromagnetic recording layer is provided between said common electrode and said non-magnetic space layer.

9. The MRAM unit as claimed in claim 1, wherein an electrically insulating confinement layer comprising a plurality of openings corresponding to said plurality of contacts is provided between said common memory block and said plurality of contacts.

10. The MRAM unit as claimed in claim 1, wherein said ferromagnetic recording layer is a synthetic antiferromagnetic pinned multi-layer comprising at least two antiferromagnetically coupled ferromagnetic layers pinned by an antiferromagnetic (AFM) layer.

11. The MRAM unit as claimed in claim 1, wherein said ferromagnetic recording layer is a hard magnetic layer.

12. The MRAM unit as claimed in claim 1, wherein said ferromagnetic recording layer is a ferromagnetic layer coupled with a hard magnetic layer.

13. The MRAM unit as claimed in claim 1, wherein said common memory block further comprises a template layer next to said plurality of contacts and a cap layer next to said common electrode.

14. The MRAM unit as claimed in claim 13, wherein at least one of said template layer, said cap layer and said free magnetic layer is a multi-synthetic ferrimagnetic layer.

15. The MRAM unit as claimed in claim 1, wherein said plurality of contacts is arranged in form of an array.

16. The MRAM unit as claimed in claim 6, wherein said common digital line is adapted to cause a magnetic field in said ferromagnetic recording layer at an activated one of said effective magnetoresistive elements upon a current passing through said common digital line.

17. The MRAM unit as claimed in claim 1, further comprising in each case a heat element adjacent to each effective magnetoresistive element.

18. The MRAM unit as claimed in claim 1, wherein said common memory block is a stacked current-perpendicular-to-plane (CPP) structure such as a magnetic tunnel junction (MTJ) or a CPP spin-valve (SV).

19. A method of writing data in a MRAM unit which comprises a plurality of transistors on a substrate, each of said plurality of transistors being a field-effect transistor and comprising first and second source/drain electrodes and a gate electrode, a plurality of active areas defined in a common memory block which is electrically connected to each of said first source/drain electrodes through in each case one of a plurality of contacts, a common electrode electrically contacting said plurality of contacts through said common memory block, and a common digital line provided electrically isolated next to said common electrode on an opposite side of said common electrode with respect to said common memory block, said

common memory block comprising a ferromagnetic recording layer, a free magnetic reading layer, a non-magnetic space layer between said ferromagnetic recording layer and said free magnetic reading layer ~~and a plurality of active areas defined in said common memory block~~, said method comprising:

controlling said plurality of transistors for electrically activating a corresponding one of said plurality of contacts, thereby electrically activating a respective active area of said plurality of active areas, said activated respective active area serving as effective magnetoresistive element;

raising the temperature of said ferromagnetic recording layer at said effective magnetoresistive element to approach or exceed its critical temperature independently of other active areas, thereby reducing the coercitivity of said ferromagnetic recording layer at said effective magnetoresistive element; and

writing a magnetization state representing a bit of said data in said ferromagnetic recording layer at said effective magnetoresistive element by passing a current through said common digital line.

20. The method according to claim 19, further comprising cooling down said ferromagnetic recording layer at said effective magnetoresistive element to nearly ambient temperature after writing said magnetization state in said ferromagnetic recording layer at said effective magnetoresistive element.

21. The method according to claim 19, wherein raising the temperature of said ferromagnetic recording layer at said effective magnetoresistive element to above its critical temperature independently of other active areas further comprises passing a heating current partly through said common electrode, completely through said effective magnetoresistive element, completely through said activated corresponding one of said plurality of contacts and completely through said controlled one of said plurality of transistors via said corresponding first and second source/drain electrodes.

22. The method according to claim 21, further comprising passing said heating current through a heat element being thermally coupled to said effective magnetoresistive element.

23. The method according to claim 21, further comprising electrically confining said heating current by means of providing an electrically insulating confinement layer comprising a plurality of openings corresponding to said plurality of contacts between said common memory block and said plurality of contacts.

24. The method according to claim 19, wherein controlling said plurality of transistors comprises applying a control voltage to said gate electrode of a respective one of said plurality of transistors and applying a voltage difference to said first and second source/drain electrodes of said respective one of said plurality of transistors.

25. A method of performing a read operation in a MRAM unit which comprises a plurality of transistors on a substrate, each of said plurality of transistors being a field-effect transistor and comprising first and second source/drain electrodes and a gate electrode, a plurality of active areas defined in a common memory block which is electrically connected to each of said first source/drain electrodes through in each case one of a plurality of contacts, a common electrode electrically contacting said plurality of contacts through said common memory block, and a common digital line provided electrically isolated next to said common electrode on an opposite side of said common electrode with respect to said common memory block, said common memory block comprising a ferromagnetic recording layer, a free magnetic reading layer, a non-magnetic space layer between said ferromagnetic recording layer and said free magnetic reading layer ~~and a plurality of active areas defined in said common memory block,~~ said method comprising:

controlling said plurality of transistors for electrically activating a corresponding one of said plurality of contacts, thereby electrically activating a respective active area of said plurality of active areas, said activated respective active area serving as effective magnetoresistive element;

applying a current through said common digital line, thereby adjusting all magnetization states in said free magnetic reading layer; and

determining the magnetization state of said ferromagnetic recording layer at said effective magnetoresistive element, wherein the resistance states of said

ferromagnetic recording layer at said effective magnetoresistive element are dependent on the relative angles between the magnetization vectors of said ferromagnetic recording layer at said effective magnetoresistive element and of said free magnetic reading layer.

26. The method according to claim 25, wherein controlling said plurality of transistors comprises applying a control voltage to said gate electrode of a respective one of said plurality of transistors and applying a voltage difference to said first and second source/drain electrodes of said respective one of said plurality of transistors.